WHAT IS CLAIMED IS:

1. A Magnetic random access memory (MRAM), comprising:

a first wiring through which a write current is caused to flow in one direction;

a selecting transistor connected to the first wiring for controlling the write current; and

a plurality of magnetic memory cells each arranged on an upstream side with respect to the position of the first wiring where the selecting transistor is provided, one ends of the plurality of magnetic memory cells being connected to the first wiring.

2. The memory as claimed in 1, wherein the other ends of the plurality of MRAM cells are connected to a second wiring through which a current is caused to flow in both directions.

3. The memory as claimed in claim 2, wherein the first wiring is a first sub-wiring, and the first sub-wiring is connected to a first main wiring directly, not through a transistor, and the second wiring is a second sub-wiring, and the second sub-wiring is connected to a second main wiring through a transistor.

4. A MRAM, comprising:

a main bit line;

a sub-bit line having one ends connected to said main bit line;

a main word line;

a sub-word line having one ends connected to said main word line;

a MRAM cell provided between said sub-word line and said sub-bit line; and

a select transistor coupled to the other end of one of said sub-word and said sub-bit lines.

5. The MRAM as claimed in claim 4, wherein a substrate current of said select transistor becomes a write current which flows through one of the sub-bit line and the sub-word line.

6. The MRAM as claimed in claim 5, wherein the substrate current is based on a snap back phenomenon which is caused to occur by applying a breakdown voltage to a drain of said select transistor.

7. The MRAM as claimed in claim 5, wherein the write current is a current generated when the electric charge accumulated in electrostatic capacity is discharged, which accompanies one of said main bit and sub-bit lines and said main word and sub-word lines.

8. A MRAM, comprising:

a plurality of first sub-row lines extending in a first direction;

a plurality of first sub-column lines extending in a second direction different from the first direction;

a first memory cell array including a plurality of first

magnetic memory cells each arranged at crossing points between a corresponding one of said first sub-row lines and a corresponding one of said first sub-column lines;

a plurality of second sub-row lines extending in the first direction;

a plurality of second sub-column lines extending in the second direction;

a second memory cell array including a plurality of second magnetic memory cells each arranged at crossing points between a corresponding one of said second sub-row lines and a corresponding one of said second sub-column lines;

a plurality of third sub-row lines extending in the first direction;

a plurality of third sub-column lines extending in the second direction;

a third memory cell array including a plurality of third magnetic memory cells each arranged at crossing points between a corresponding one of said third sub-row lines and a corresponding one of said third sub-column lines;

a plurality of main row lines provided in common to said first and second memory cell arrays; and

a plurality of main column lines provided in common to aid first and third memory cell arrays,

wherein each of the plurality of sub-row lines of the first memory cell array has two end portions, and one of the two end portions is connected to one of the main lines, and the other end portion of the two end portions is connected to a first row selecting transistor, and

each of the plurality of sub-column lines of the first memory cell array has two end portions, and one of the two end portions is connected to one of the main column lines through a column selecting transistor, and the other end portion of the two end portions is connected to a write circuit.

9. The MRAM as claimed in claim 8, wherein a predetermined write current caused to flow through one of the sub-row lines during a write operation is a current generated when a predetermined signal is supplied to a row selecting signal line of the row selecting transistors to make one of the row selecting transistors get a conducting state to discharge the electric charge previously accumulated in electrostatic capacity of one of the main row lines and the sub-row lines.

10. The MRAM as claimed in claim 9, wherein the conducting state of the row selecting transistor is a state in which a current is caused to flow from a drain of the row selecting transistor to a substrate.

11. A data writing method for an MRAM, wherein data is written to a selected tunneling magneto-resistance (TMR) cell using a snap back current.

12. The data writing method as claimed in claim 11, wherein a plurality of TMR cells each is coupled between a common sub word line, a write current corresponding to said snap back current is in said sub word line.

13. The data writing method as claimed in claim 12, wherein a MOS transistor provided at a down stream side of said sub word line with respect to said selected TMR cell and MOS transistor is operated so as to produce said snap back current.

14. The data writing method as claimed in claim 13, wherein a current for writing said data into said selected TMR cell flows from a main word line to said sub word line without flowing through a transistor.

15. The data writing method as claimed in claim 14, wherein before said write current flows in the selected TMR cell, electric charge is accumulated in at least the main word line.

16. The data writing method as claimed in claim 15, said electric charge is accumulated in the sub word line.

17. A data writing method for an MRAM, comprising:

accumulating the electric charges in an electrostatic capacity of one of word and bit lines; and

discharging the accumulated electric charges to produce a discharge current to write data to a selected TMR cell.

18. The data writing method as claimed in claim 17, wherein said electric charge is accumulated in a main word line and sub word line.

19. The data writing method as claimed in claim 18, wherein said electric charge is discharged by snap back phenomenon.

20. The data writing method as claimed in claim 19, wherein a voltage which does not cause said snap back phenomenon is supplied non selected TMR cells.